

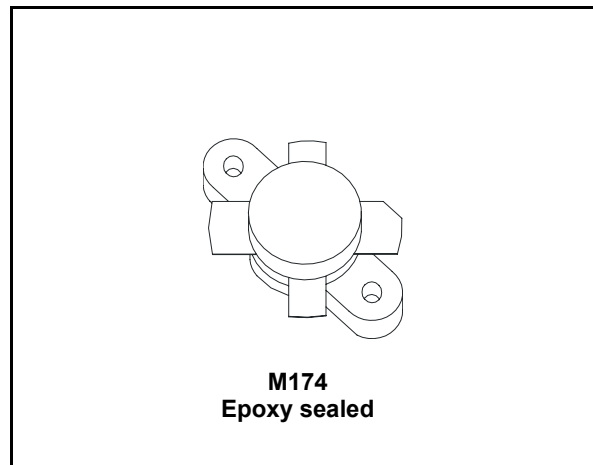
### Features

- Gold metallization
- Excellent thermal stability
- Common source configuration
- $P_{OUT} = 150\text{ W min. with } 14\text{ dB gain @ } 175\text{ MHz}$
- Thermally enhanced packaging for lower junction temperatures

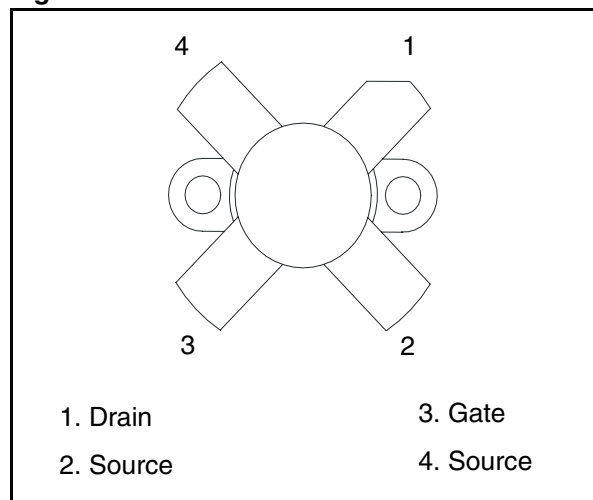
### Description

The SD2931-10 is a gold metallized N-channel MOS field-effect RF power transistor. Being electrically identical to the standard SD2931 MOSFET, it is intended for use in 50 V dc large signal applications up to 230 MHz.

The SD2931-10 is mechanical compatible to the SD2931 but offers in addition a better thermal capability (25 % lower thermal resistance), representing the best-in-class transistors for ISM applications, where reliability and ruggedness are critical factors.



**Figure 1. Pin connection**



**Table 1. Device summary**

Order code	Marking	Package	Packaging
SD2931-10	SD2931-10	M174	Plastic tray

# Contents

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# 1 Electrical data

## 1.1 Maximum ratings

**Table 2. Absolute maximum ratings** ( $T_{CASE} = 25\text{ °C}$ )

Symbol	Parameter	Value	Unit
$V_{(BR)DSS}^{(1)}$	Drain source voltage	125	V
$V_{DGR}$	Drain-gate voltage ( $R_{GS} = 1\text{ M}\Omega$ )	125	V
$V_{GS}$	Gate-source voltage	$\pm 20$	V
$I_D$	Drain current	20	A
$P_{DISS}$	Power dissipation	389	W
$T_J$	Max. operating junction temperature	200	$^{\circ}\text{C}$
$T_{STG}$	Storage temperature	-65 to +150	$^{\circ}\text{C}$

1.  $T_J = 150^{\circ}\text{C}$

## 1.2 Thermal data

**Table 3. Thermal data**

Symbol	Parameter	Value	Unit
$R_{thJC}$	Junction - case thermal resistance	0.45	$^{\circ}\text{C/W}$

## 2 Electrical characteristics (T<sub>CASE</sub> = +25 °C)

### 2.1 Static

Table 4. Static (per side)

Symbol	Test conditions			Min	Typ	Max	Unit
V <sub>(BR)DSS</sub>	V <sub>GS</sub> = 0 V	I <sub>DS</sub> = 100 mA		125			V
I <sub>DSS</sub>	V <sub>GS</sub> = 0 V	V <sub>DS</sub> = 50 V				50	μA
I <sub>GSS</sub>	V <sub>GS</sub> = 20 V	V <sub>DS</sub> = 0 V				250	nA
V <sub>GS(Q)</sub> <sup>(1)</sup>	V <sub>DS</sub> = 10 V	I <sub>D</sub> = 250 mA		See table below			V
V <sub>DS(ON)</sub>	V <sub>GS</sub> = 10 V	I <sub>D</sub> = 10 A				3.0	V
G <sub>FS</sub>	V <sub>DS</sub> = 10 V	I <sub>D</sub> = 5 A		5	6		mho
C <sub>ISS</sub>	V <sub>GS</sub> = 0 V	V <sub>DS</sub> = 50 V	f = 1 MHz		480		pF
C <sub>OSS</sub>	V <sub>GS</sub> = 0 V	V <sub>DS</sub> = 50 V	f = 1 MHz		190		pF
C <sub>RSS</sub>	V <sub>GS</sub> = 0 V	V <sub>DS</sub> = 50 V	f = 1 MHz		18		pF

1. V<sub>GS(Q)</sub> sorted with alpha/numeric code marked on unit.

### 2.2 Dynamic

Table 5. Dynamic

Symbol	Test conditions			Min	Typ	Max	Unit
P <sub>OUT</sub>	V <sub>DD</sub> = 50 V	I <sub>DQ</sub> = 250 mA	f = 175 MHz	150			W
G <sub>PS</sub>	V <sub>DD</sub> = 50 V	I <sub>DQ</sub> = 250 mA	P <sub>OUT</sub> = 150 W f = 175 MHz	14	15		dB
n <sub>D</sub>	V <sub>DD</sub> = 50 V	I <sub>DQ</sub> = 250 mA	P <sub>OUT</sub> = 150 W f = 175 MHz	55	65		%
Load mismatch	V <sub>DD</sub> = 50 V	I <sub>DQ</sub> = 250 mA	P <sub>OUT</sub> = 150 W f = 175 MHz All phase angles	10:1			VSWR

Table 6. V<sub>GS</sub> sorts

A	2.0 - 2.1	K	2.9 - 3.0
B	2.1 - 2.2	L	3.0 - 3.1
C	2.2 - 2.3	M	3.1 - 3.2
D	2.3 - 2.4	N	3.2 - 3.3
E	2.4 - 2.5	P	3.3 - 3.4
F	2.5 - 2.6	Q	3.4 - 3.5
G	2.6 - 2.7	R	3.5 - 3.6
H	2.7 - 2.8	S	3.6 - 3.7
J	2.8 - 2.9		

### 3 Impedance data

Figure 2. Impedance data

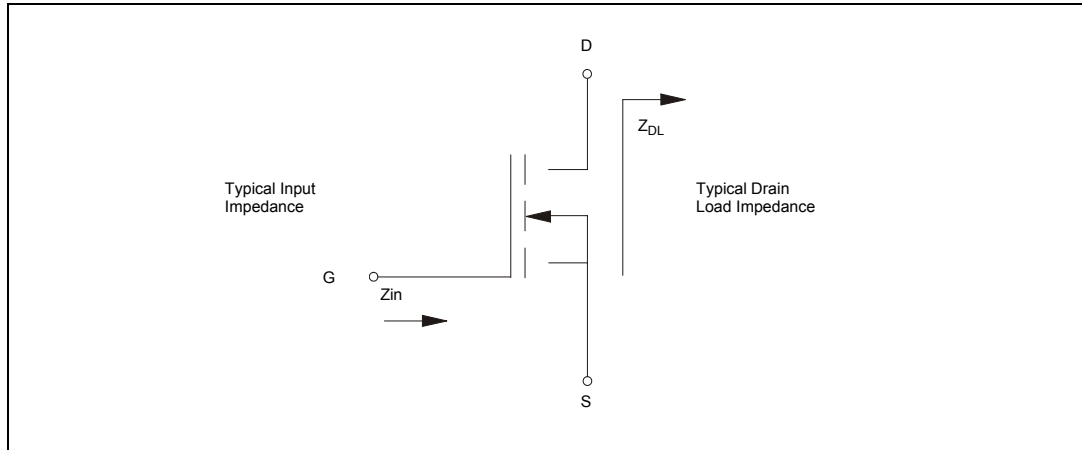
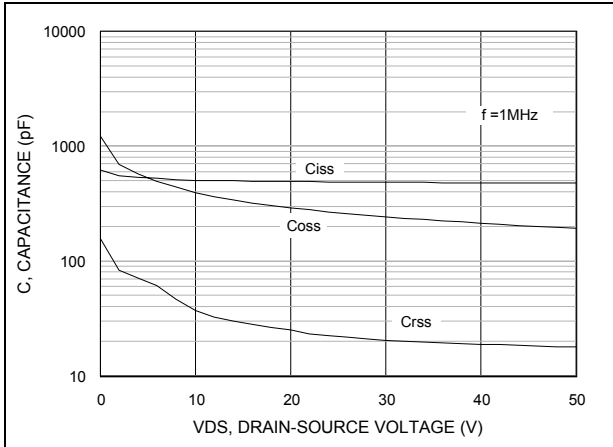


Table 7. Impedance data

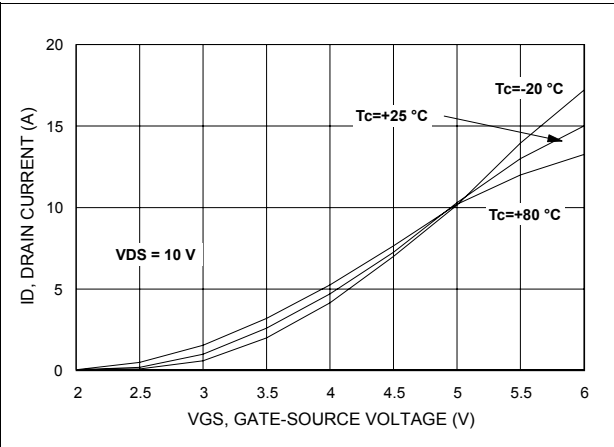
Freq	$Z_{IN}$ ( $\Omega$ )	$Z_{DL}$ ( $\Omega$ )
30 MHz	$1.7 - j 5.7$	$6.8 + j 0.9$
175 MHz	$1.2 - j 2.0$	$2.0 + j 2.4$

# 4 Typical performance

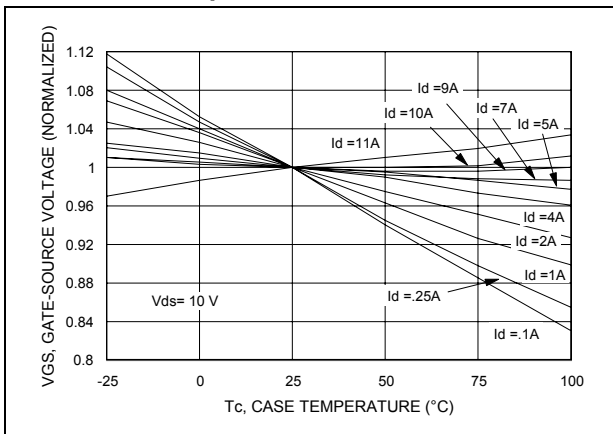
**Figure 3. Capacitance vs drain-source voltage**



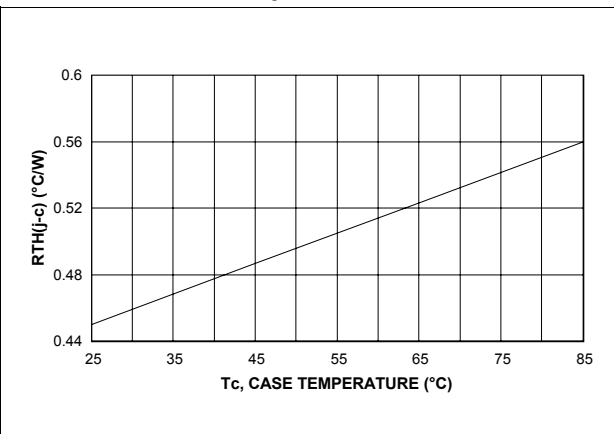
**Figure 4. Drain current vs gate voltage**



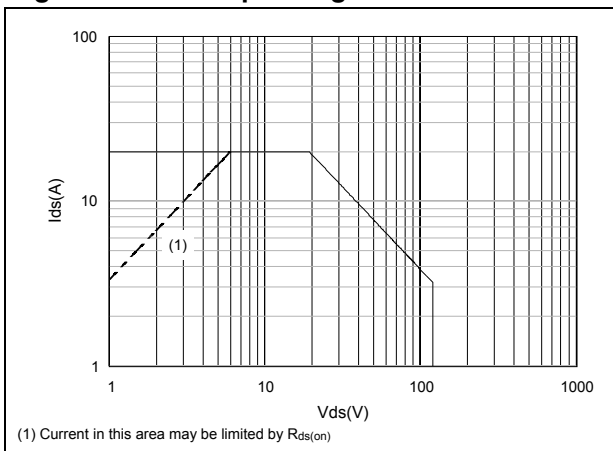
**Figure 5. Gate-source voltage vs case temperature**



**Figure 6. Maximum thermal resistance vs case temperature**



**Figure 7. Safe operating area**



## 5 Typical performance 175 MHz

Figure 8. Output power vs input power

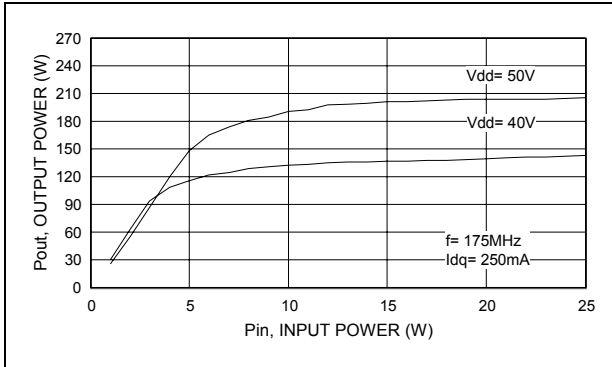


Figure 9. Output power vs input power

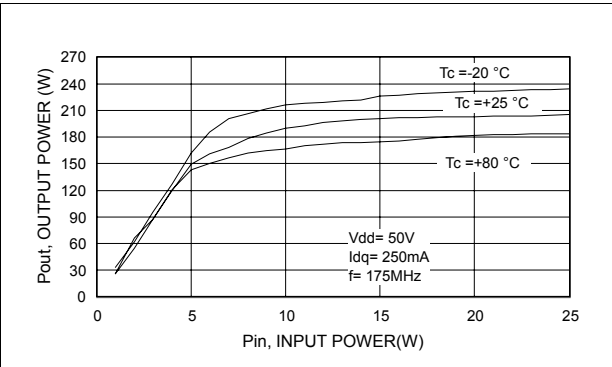


Figure 10. Power gain vs output power

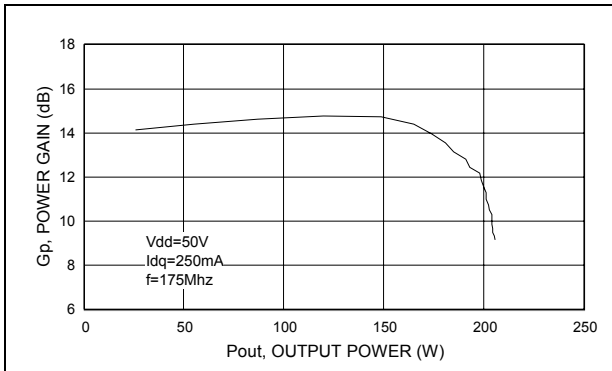


Figure 11. Efficiency vs output power

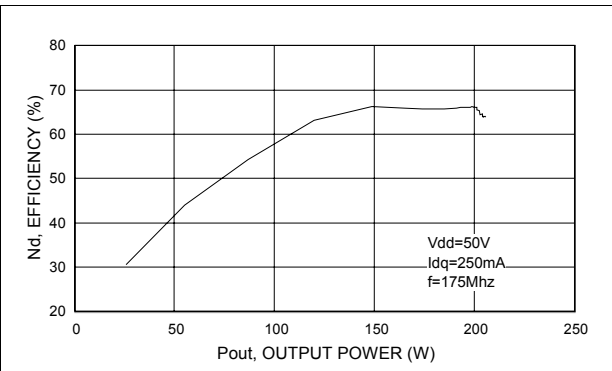


Figure 12. Output power vs supply voltage

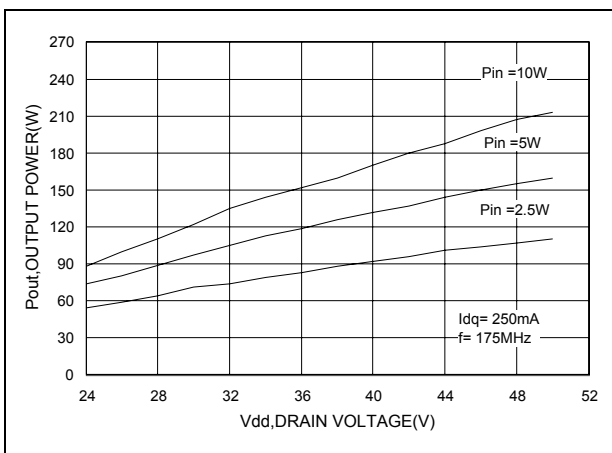
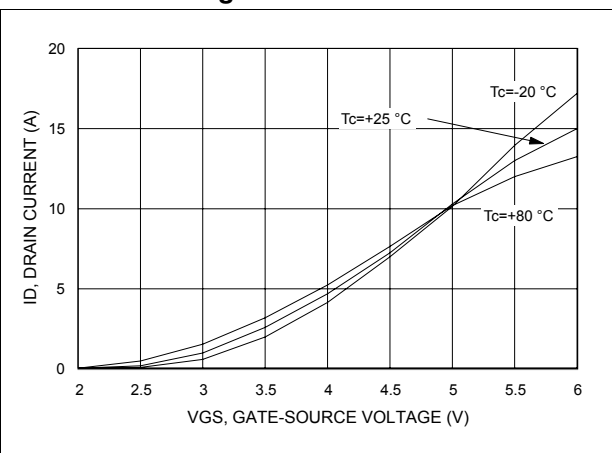


Figure 13. Drain current vs gate-source voltage



## 6 Test circuit

Figure 14. 175 MHz test circuit schematic (production test circuit)

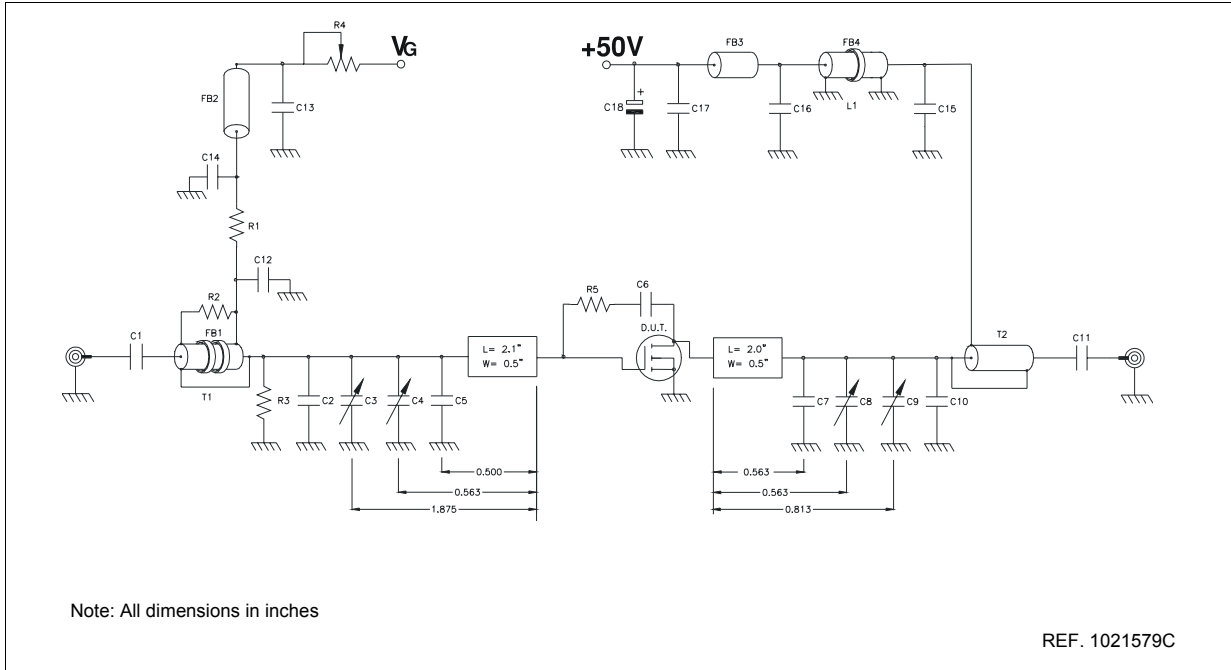


Table 8. Component part list

Component	Description
T1	4:1 transformer, 25 ohm flexible coax .090 OD 6" long
T2	1:4 transformer, 25 ohm semi-rigid coax .141 OD 6" long
FB1	Toroid X 2, 0.5" OD .312" ID 850 $\mu$ 2 turns
FB2, FB3	VK200
FB4	Shield bead, 1" OD 0.5" ID 850 $\mu$ 3 turns
L1	1/4 wave choke, 50 ohm semi-rigid coax .141 OD 12" Long
PCB	0.62" woven fiberglass, 1 oz. copper, 2 sides, $\epsilon_r = 2.55$
R1, R3	470 ohm 1 W chip resistor
R2	360 ohm 1/2 W resistor
R4	20 Kohm 10 turn potentiometer
R5	560 ohm 1 W resistor
C1, C11	470 pF ATC chip cap
C2	43 pF ATC chip cap
C3, C8, C9	Arco 404, 12-65 pF
C4	Arco 423, 16-100 pF



**Table 8. Component part list (continued)**

Component	Description
C5	120 pF ATC chip cap
C6	0.01 $\mu$ F ATC chip cap
C7	30 pF ATC chip cap
C10	91 pF ATC chip cap
C12, C15	1200 pF ATC chip cap
C13, C14, C16, C17	0.01 $\mu$ F / 500 V chip cap
C18	10 $\mu$ F 63 V electrolytic capacitor

**Figure 15. 175 MHz test circuit photomaster**

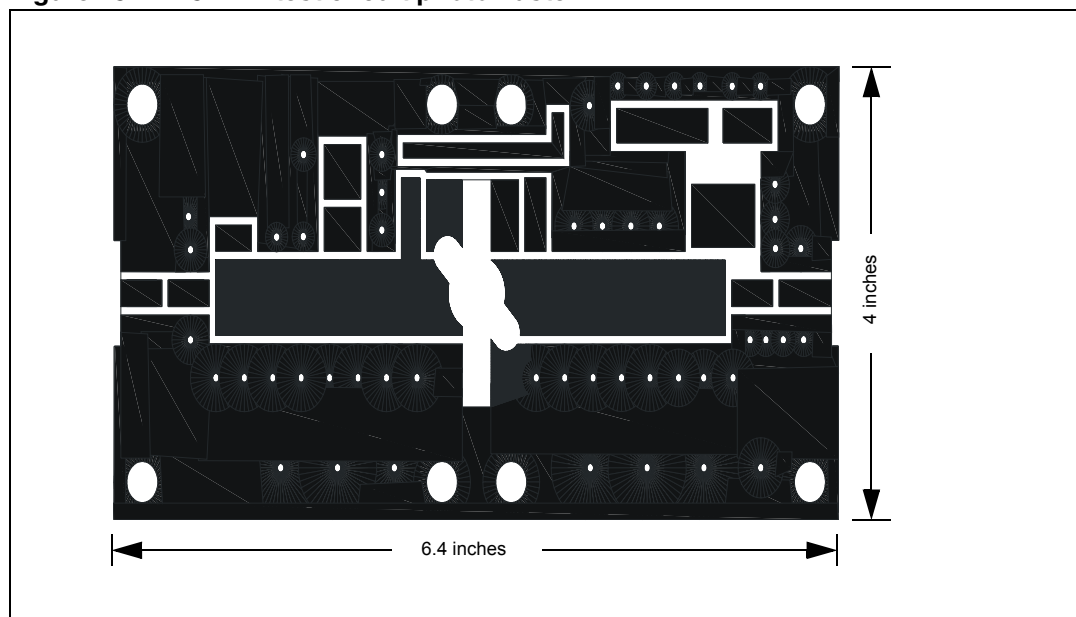
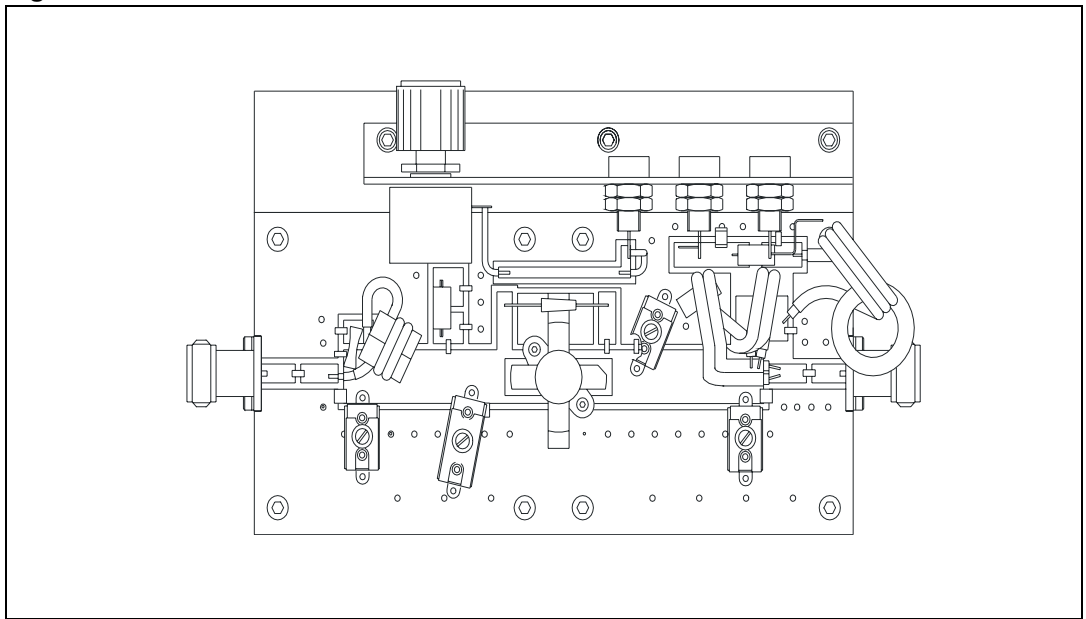
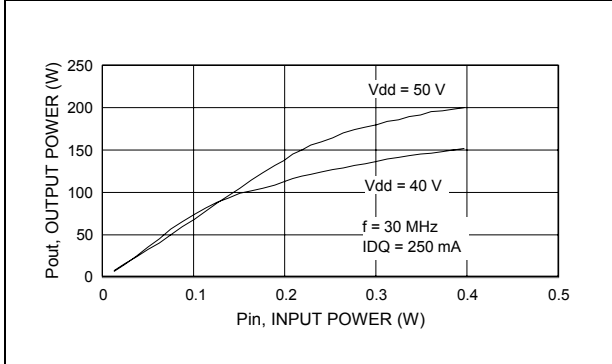


Figure 16. 175 MHz test circuit

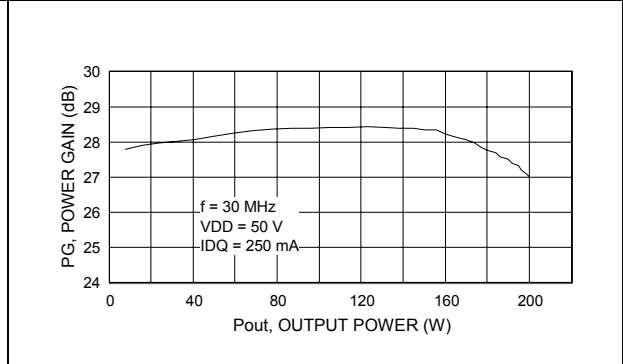


# 7 Typical performance 30 MHz

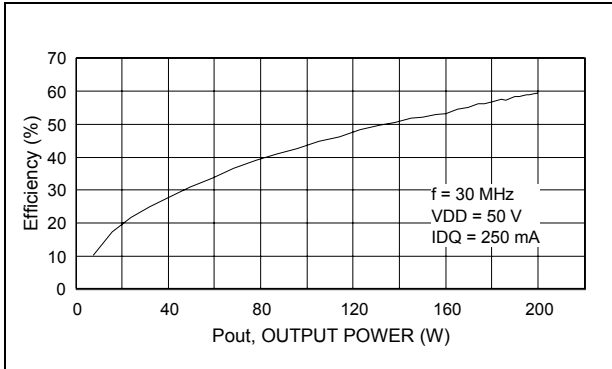
**Figure 17. Output power vs input power**



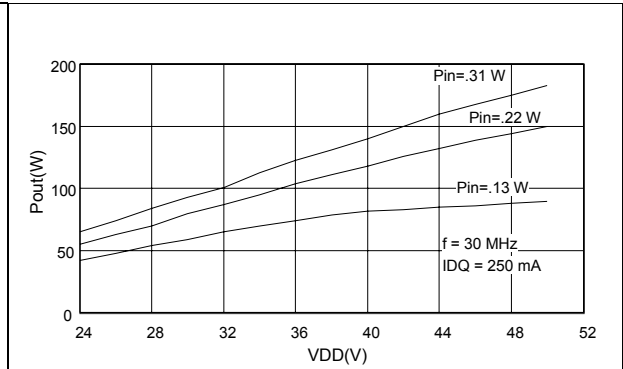
**Figure 18. Power gain vs output power**



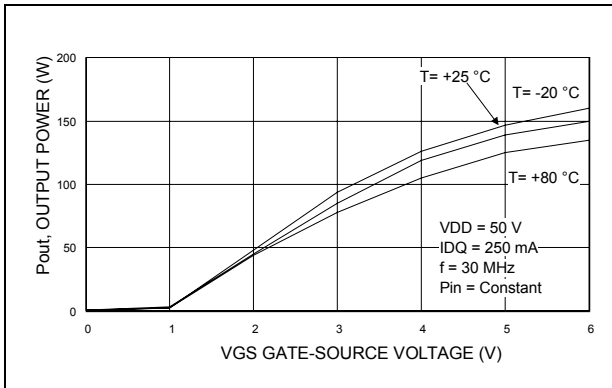
**Figure 19. Efficiency vs output power**



**Figure 20. Output power vs supply voltage**



**Figure 21. Output power vs gate voltage**



# 8 Test circuit 30 MHz

Figure 22. 30 MHz test circuit schematic (engineering test circuit)

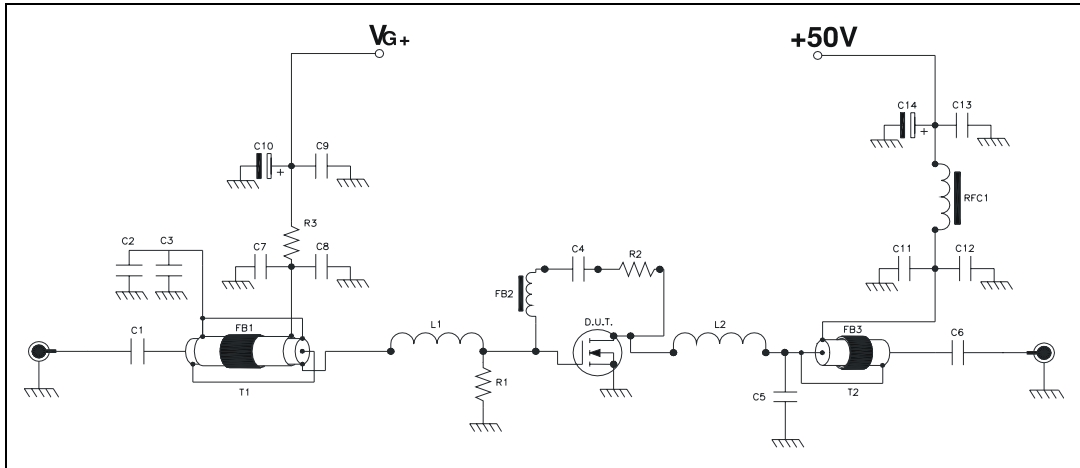


Figure 23. 30 MHz test circuit component part list

Symbol	Description
T1	9:1 transformer, 25 Ω flexible coax with extra shield .090 OD 15" long
T2	1:4 transformer, 50 Ω flexible coax .225 OD 15" long
FB1	Toroid 1.7" OD .30" ID 220 μ 4 turns
FB2	Surface mount EMI shield bead
FB3	Toroid 1.7" OD .300" ID 220μ 3 turns
RFC1	Toroid 0.5" OD 0.30" ID 125μ 4 turns 12 awg wire
PCB	0.62" Woven Fiberglass, 1 oz. Copper, 2 Sides, εr = 2.55
R1, R3	1 KΩ 1 W chip resistor
R2	680 Ω 3 W wirewound resistor
C1,C4,C6,C7,C8,C9, C11,C12,C13	0.1 μF ATC chip cap
C2,C3	750 pF ATC chip cap
C5	470 pF ATC chip cap
C10	10 μF 63 V electrolytic capacitor
C14	100 μF 63 V electrolytic capacitor

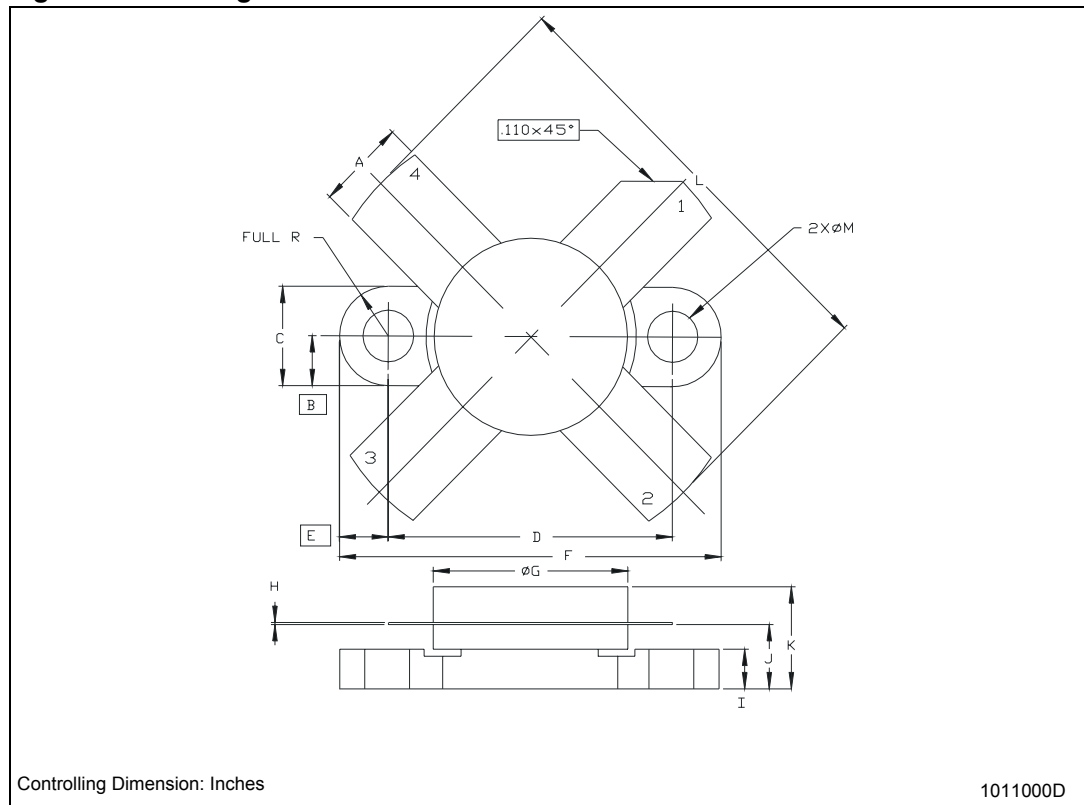
## 9 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK<sup>®</sup> packages. These packages have a lead-free second level interconnect. The category of second Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: [www.st.com](http://www.st.com).

**Table 9. M174 (0.500 DIA 4/L N/HERM W/FLG) mechanical data**

Dim.	mm.			Inch		
	Min	Typ	Max	Min	Typ	Max
A	5.56		5.584	0.219		0.230
B		3.18			0.125	
C	6.22		6.48	0.245		0.255
D	18.28		18.54	0.720		0.730
E		3.18			0.125	
F	24.64		24.89	0.970		0.980
G	12.57		12.83	0.495		0.505
H	0.08		0.18	0.003		0.007
I	2.11		3.00	0.083		0.118
J	3.81		4.45	0.150		0.175
K			7.11			0.280
L	25.53		26.67	1.005		1.050
M	3.05		3.30	0.120		0.130

**Figure 24. Package dimensions**



## 10 Revision history

**Table 10. Document revision history**

<b>Date</b>	<b>Revision</b>	<b>Changes</b>
09-Sep-2004	4	
17-Jun-2004	5	Updated <i>Table 5: Dynamic on page 4</i>
04-Mar-2008	6	Updated <i>Table 4: Static (per side)</i> , <i>Table 5: Dynamic</i> and <i>Table 6: VGS sorts on page 4</i>

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